Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The new title better reflects the claimed subject matter.

Canceling claims 1-14 overcomes the rejection under 35 USC 112.

Amended claim 15 better particularly points out and distinctly claims the subject matter the applicant regards as his invention.

New claim 15 defines an integrated circuit comprising a semiconductor substrate, functional IP core circuits formed on the substrate, and test circuits formed on the substrate within the periphery of the functional IP core circuits.

The functional IP core circuits form a periphery on the substrate and have functional core input leads and functional core output leads that extend beyond that periphery.

The test circuits include a test data input lead, a test data output lead, a test clock lead, and a test mode select lead, all extending beyond the periphery of the functional IP core circuits.

The test circuits include a test access port coupled to the test data input lead, the test data output lead, the test clock lead, and the test mode select lead.

The test circuits include test data registers coupled to the test data input lead, the test data output lead, the test clock lead, and the test mode select lead.

The test circuits include an instruction register coupled to the test data input lead and the test data output lead.

The test circuits include an external register present lead connected to the instruction register and extending beyond the periphery of the functional IP core circuits.

In contrast to Applicant's admitted prior art, present claim 15 requires that the test circuits include an external register present lead connected to the instruction register and extending beyond the periphery of the functional IP core circuits.

The patent to West, US 6,173,428, discloses an ASIC integrated circuit 20 with device logic 22 and test logic 30. Logic 30 is boundary scan logic designed in accordance with an IEEE/ANSI 1149.1-1990 standard.

The test logic 30, Figure 4, includes user-defined registers 40 allowed under the standard.

Figure 5 depicts inputs to the TAP Controller Logic and outputs from the TAP Controller Logic. One of the outputs is called ENABLE FOR USER DEF. REGISTERS.

In this context, the West patent apparently provides functional IP core circuits 22 within the periphery of the input pins 24 and output pins 25, and test circuits 30 within that periphery.

In that context, the West patent fails to teach or disclose any external register present lead extending beyond the periphery of the ASIC integrated circuit 20.

Further, the West patent fails to teach or disclose connecting any external register present lead to the instruction register of the test circuits.

The claim limitation of the test circuits including an external register present lead connected to the instruction register and extending beyond the periphery of the functional IP core circuits defines over the disclosure of the West patent.

The Handly patent, US 5,862,152, discloses a JTAG module (12) including a master component (20) and any number of slave components (22). The signal INT_EXT_SEL is output from instruction register 66 to control multiplexers 60, 62, and 70 (2 places) and demultiplexer 68 (2 places). The only input depicted in Figure 2 from the slave components to the master component is the serial data input lead ISDI 43.

The Handly patent, like the West patent, fails to teach or disclose connecting any external register present lead to the instruction register of the test circuits.

The claim limitation of the test circuits including an external register present lead connected to the instruction register and extending beyond the periphery of the functional IP core circuits defines over the disclosure of the West patent.

The depending claims also are allowable as depending on allowable independent claim 15 and including limitations that distinguish over the cited art.

Claim 16 requires that the instruction register includes a capture-shift-update register section and that the external register present lead is connected to the capture-shift-update register section.

Claim 17 requires that the instruction register includes a decode section and the external register present lead is connected to the decode section.

Claim 18 requires that the instruction register includes a capture-shift-update register section and a decode section and the external register present lead is connected to the capture-shift-update register section and the decode section.

None of the West or Handly patents disclose the test circuits including an external register present lead connected to any part of the instruction register and extending beyond the periphery of the functional IP core circuits.

Claim 19 requires that the external register present lead is only an input lead that carries only an input signal. The cited art fails to disclose this feature.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,

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